A Voltage Reference Circuit in 130 nm CMOS

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Outline

- Motivation
- Circuit architecture
- Implementation
- Measurements
- Summary

Motivation

- Start to learn how to survive in the analog world with supply around 1 to 1.5 V without using thick oxide devices
- Voltage reference circuits are mandatory in:
  - Biasing circuits
  - Bus drivers
  - ADCs
  - …
- Explore possibility of implementing analog circuits in 0.13 μm CMOS without enclosed transistors

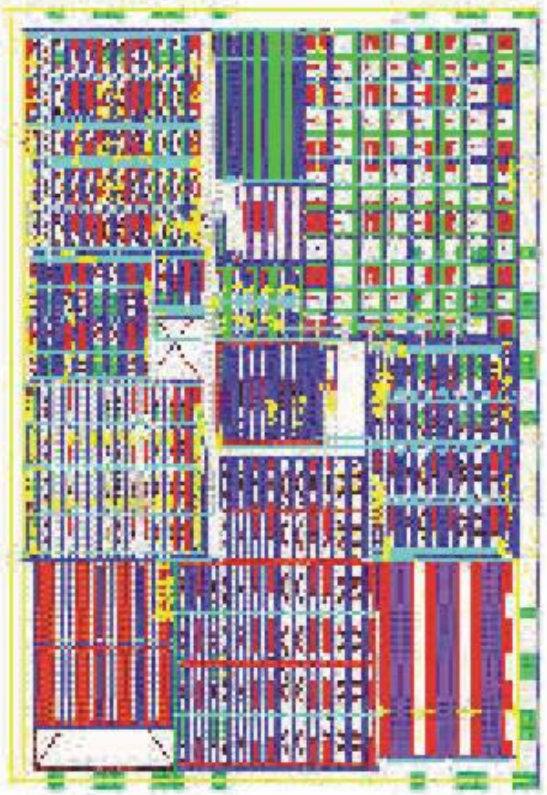
130 nm Technology features

- V_{DD} 1.2 – 1.5 V
- Tox: ~ 22 Å
- Types of devices
  - Regular FET, High V_T FET, Low V_T FET, 2.5V IO FET, Zero V_T FET
- Cu metalization
- N-well (dual well option exists)
- Metal width/pitch:
  - M1: 0.16/0.16 μm
  - M2..M5: 0.20/0.20 μm
  - LM: 0.40/0.60 μm

Reference: previous design in 0.25 μm

- Performance summary:
  - V_{out} = 1.16 V @ 25 ° C
  - V_{supply_min} = 1.2 V
  - $\Delta V_{out}/\Delta V_{supply}$ = 1mV/V
  - $\Delta V_{out}/\Delta T$ = -0.22 mV/ ° C
  - P = 62.5 mW
  - Area: 400x275 μm
  - RH: output drift
    - 0 mV @ 1 Mrad
    - 10 mV @ 10 Mrad (first version)

Corrected with new diode layout



Architecture: quick tutorial

Basic Idea:

1) Take two voltage sources with different temperature dependence

$$V_1 = V_1(T) \qquad \Delta V_1(T)/\Delta T = k_1 \cdot T + \ldots$$
$$V_2 = V_2(T) \qquad \Delta V_2(T)/\Delta T = k_2 \cdot T + \ldots$$

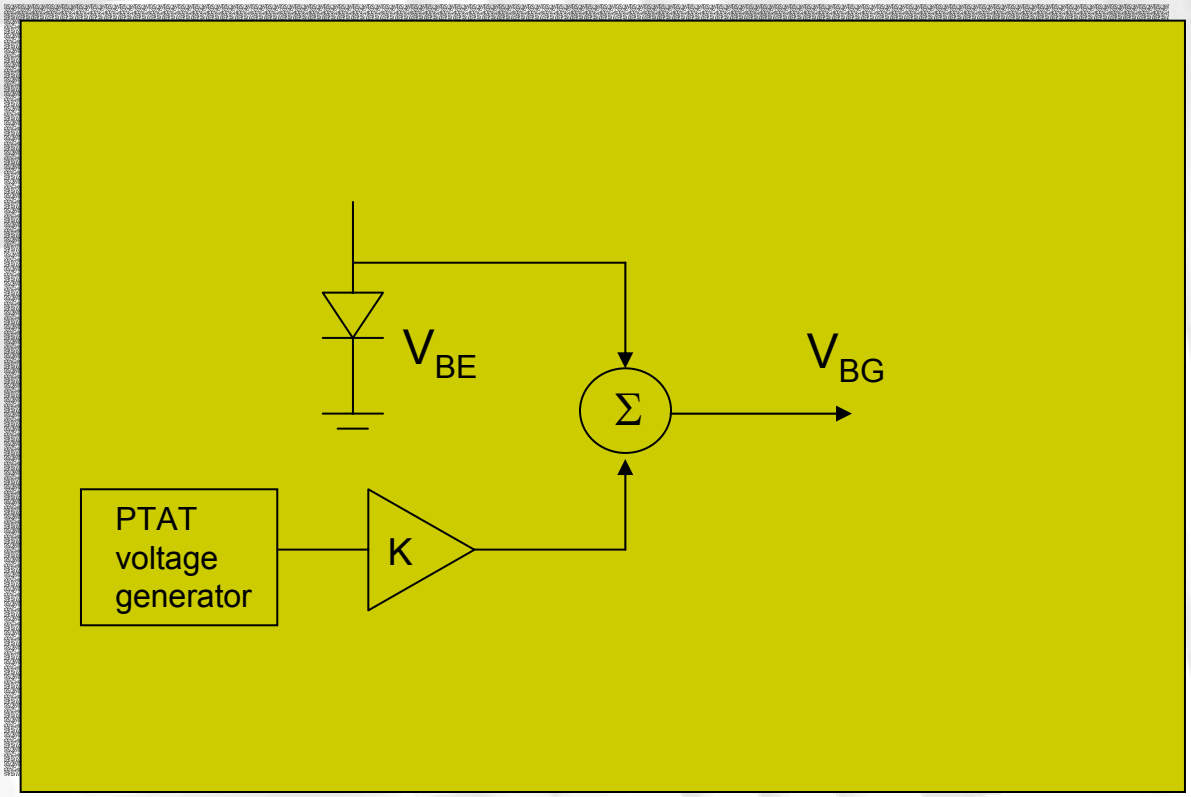
2) Combine them in a linear fashion as to obtain $\Delta V/\Delta T = 0$

$$V_{ref} = \alpha \cdot V_1(T) + \beta \cdot V_2(T)$$

choose α and β such as

$$\Delta V_{ref}/\Delta T = 0$$

Architecture: quick tutorial



The PTAT term is produced by biasing two diodes at different current densities

Architecture

$$V_{BG} = V_{BE}(T) + K \cdot V_{PTAT}(T)$$

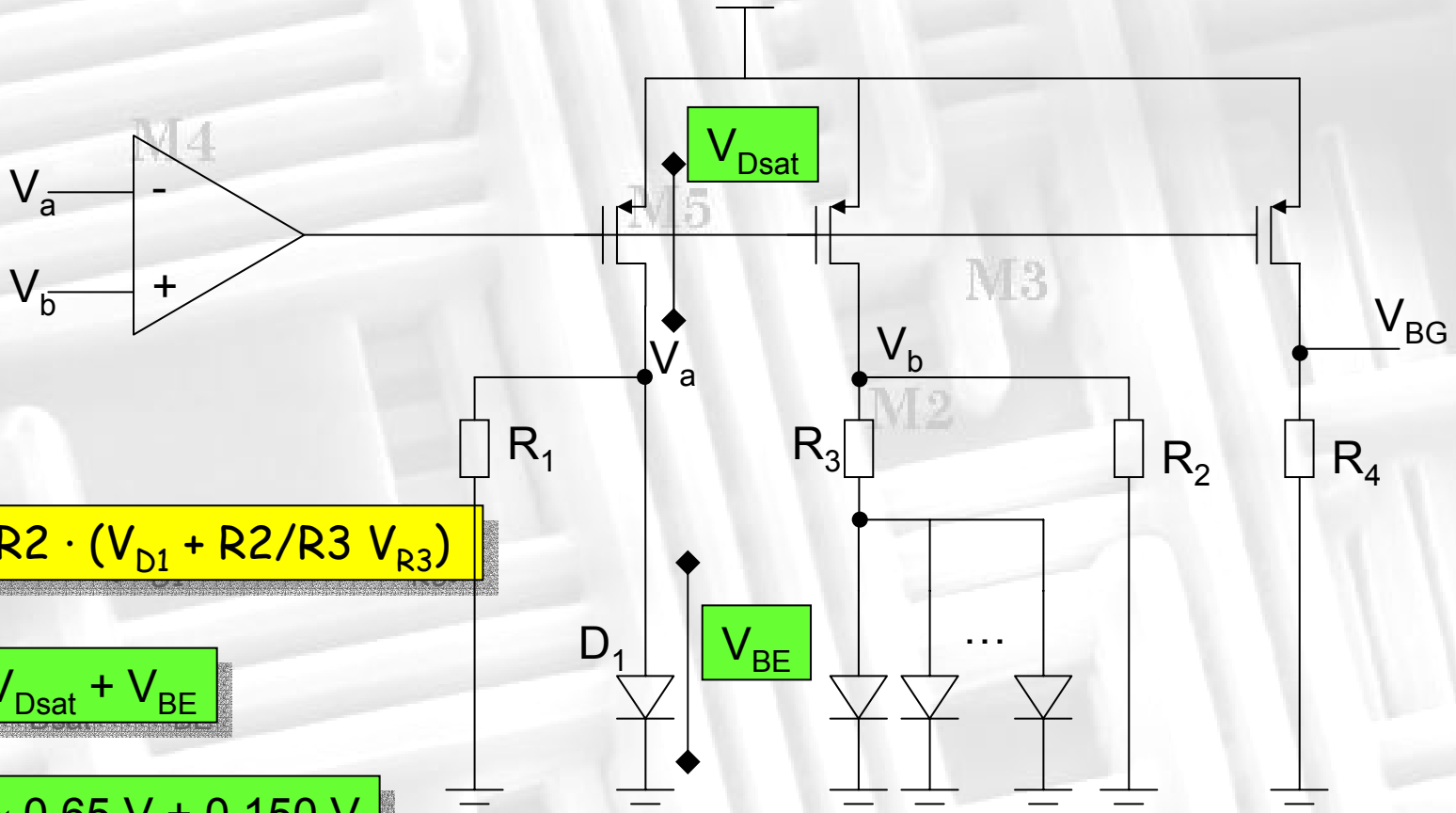
$$\Delta V_{BE}(T)/\Delta T = \sim -2\ mV/\ ^{\circ}C$$
$$\Delta V_{PTAT}(T)/\Delta T = 0.086\ mV/\ ^{\circ}C$$

➔ $K = \sim 22$

➔ $V_{BG} = \sim 1.25\ V$

- With V_{DD} @ 1.5 V and below the traditional architecture has to be modified

Low Voltage BG Reference (1)



$V_{BG} = R4/R2 \cdot (V_{D1} + R2/R3\ V_{R3})$

$V_{DDmin} = V_{Dsat} + V_{BE}$

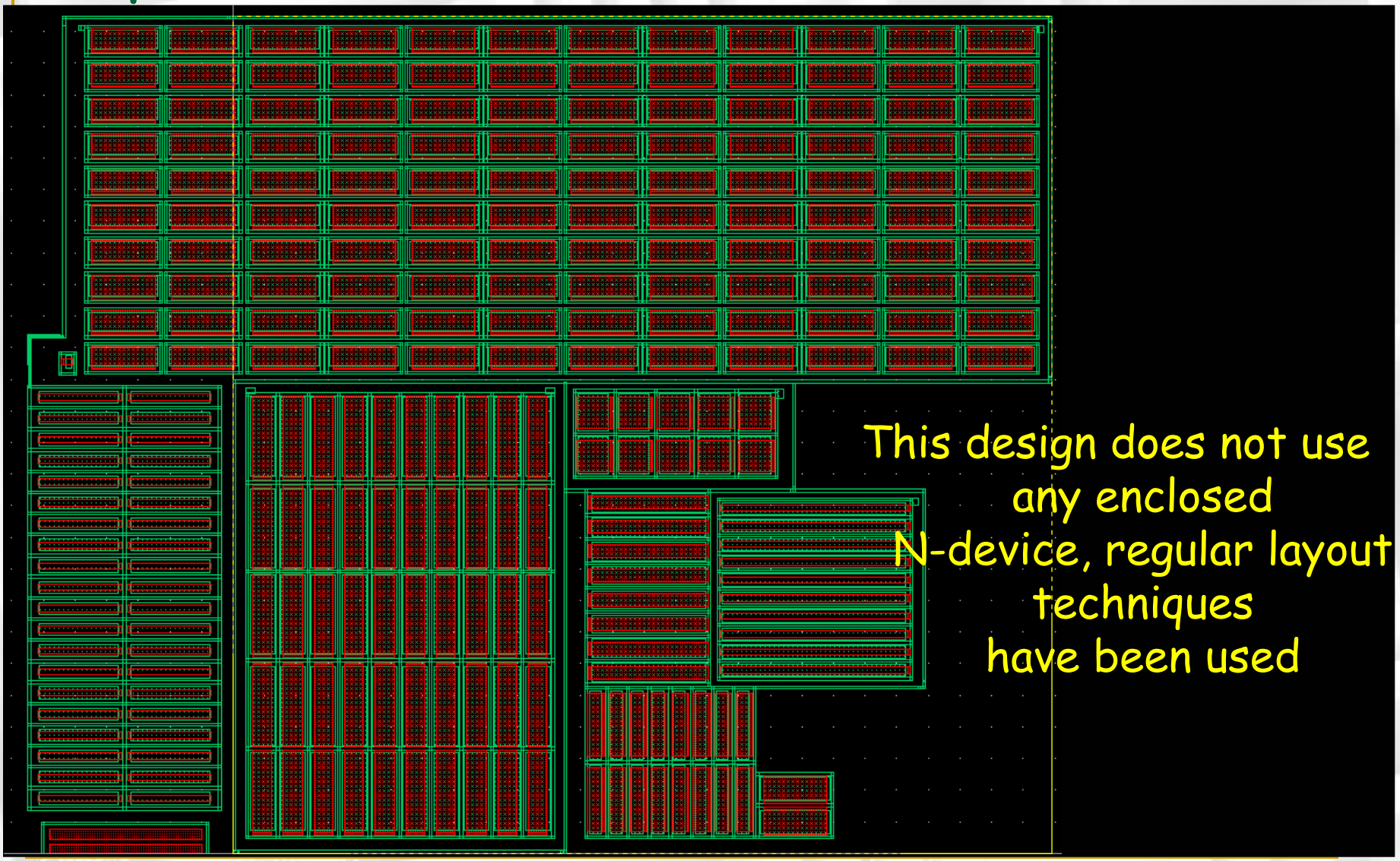
$V_{DDmin} = \sim 0.65\ V + 0.150\ V$

(1) from H. Banba et al. JSSCC, v34, n.5, May 1999

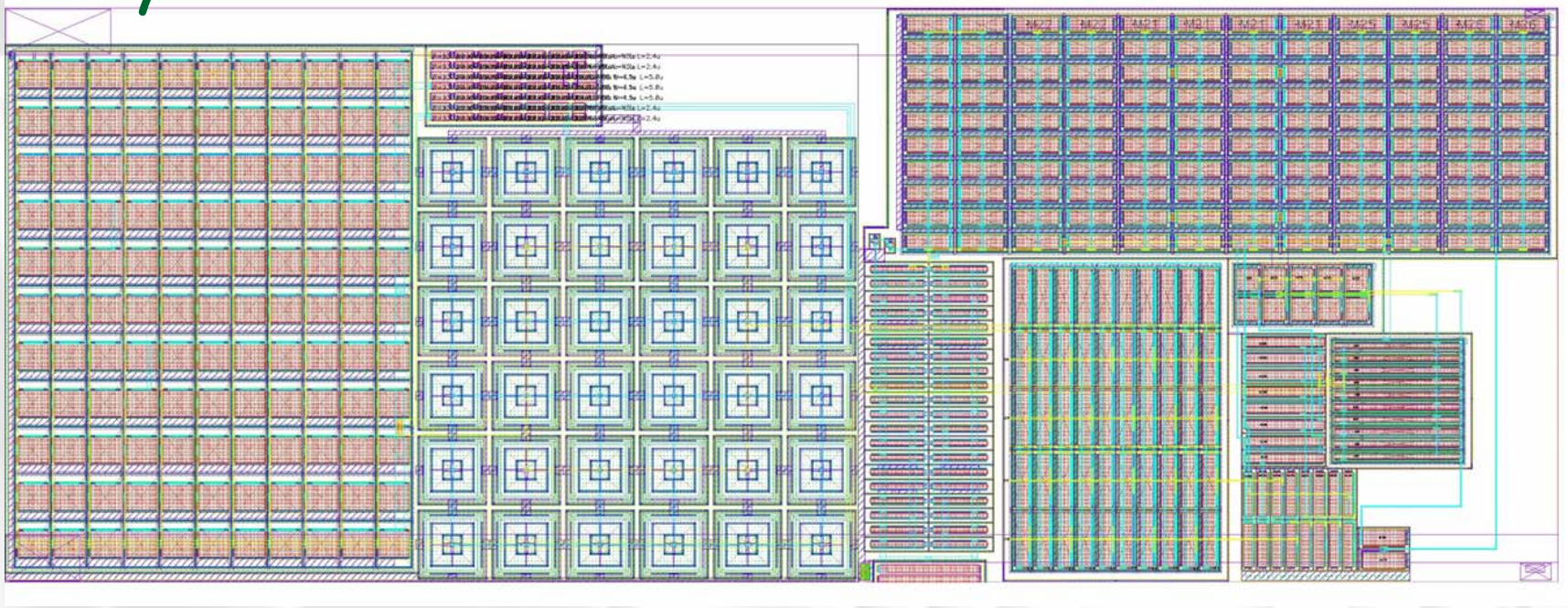
Low Voltage Bandgap Reference

- Potential problems
  - Gain
  - Offset of op-amp (measured as 0.5 mV)
  - Output range of op-amp
  - Second order effects in temperature dependence

Implementation (OP-amp, only poly and RX shown)



Layout in 130 nm

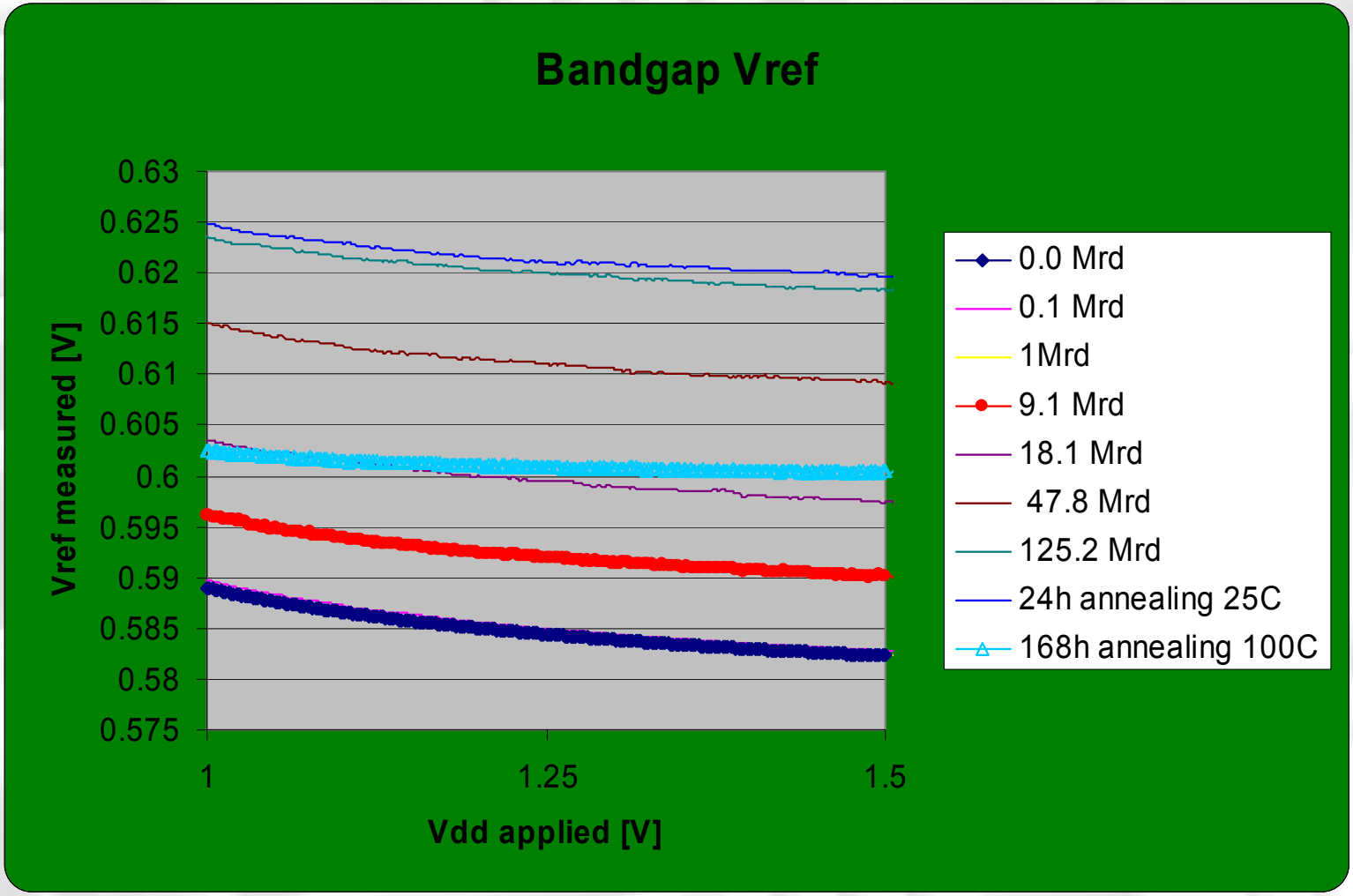


- Features :
  - V_{out} = 0.585 V @ 25 °C
  - V_{supply_min} = 1.0 V
  - Area: 360 x 130 μm
  - Supply: ~ 300 μA

Simulation and Measurement Summary

	Simulation forecast (first models)	Measured chip	Re-simulation forecast (new models)
VOut	0.589 V	0.587 V	0.589
$\Delta V_{out}/\Delta V_{supply}$	-0.49 mV/V	14 mV/V	12 mV/V
$\Delta V_{out}/\Delta T$	0.014 mV/ ° C	0.22 mV/°C	0.075 mV/°C

Irradiation of 130 nm sample (1)



Irradiation Results (2)

- Supply current:
  - Pre-irradiation:

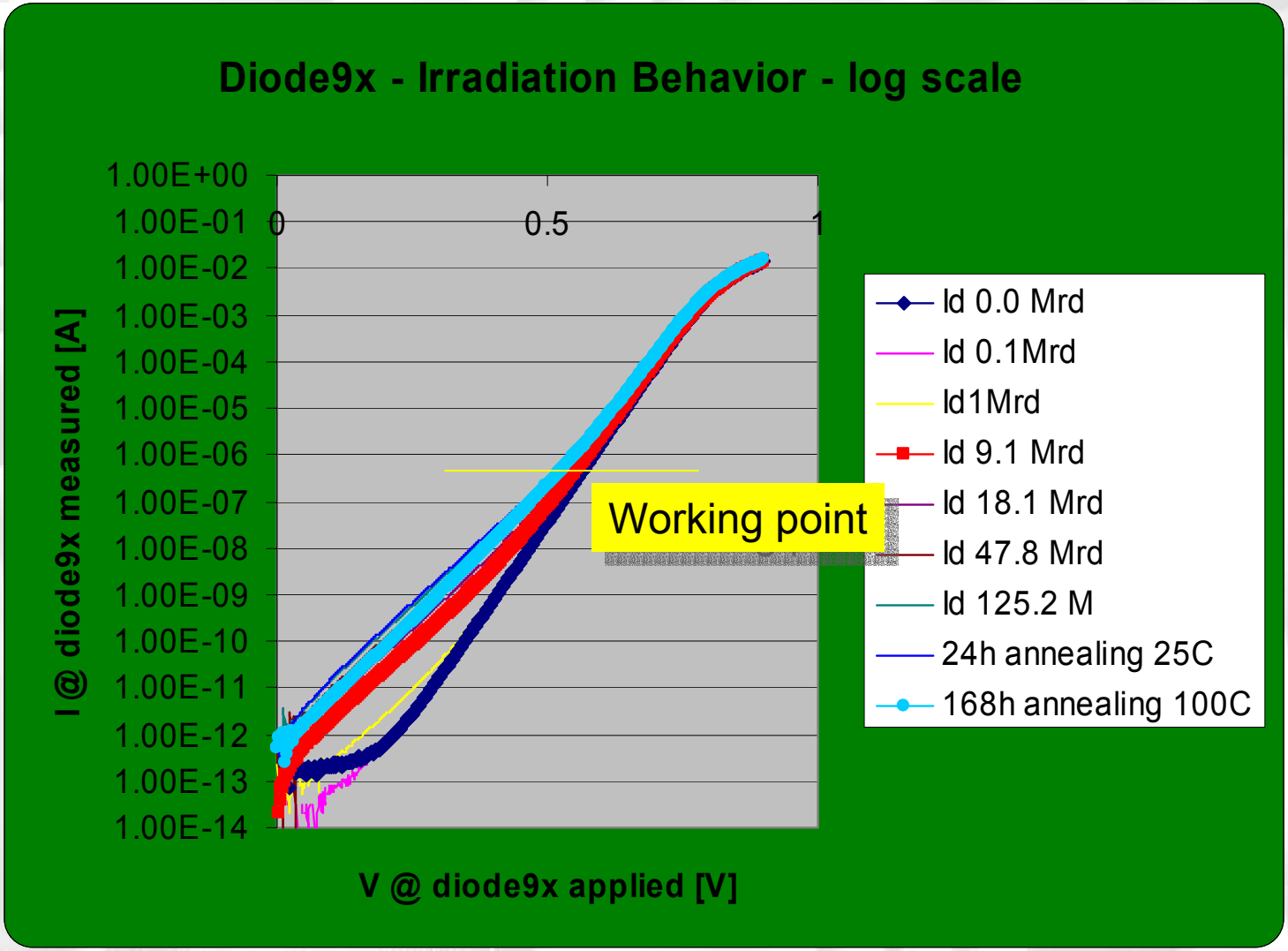
$$I_{DD} = 310\ \mu A\ @\ 1.5\ V\ ^{(1)}$$

  - After 120 Mrad + standard annealing:

$$I_{DD} = 290\ \mu A \text{ (but different device)}$$

(1) Measurement actually includes 1 full BG cell + extra test-op-amp

Irradiated Diodes behavior



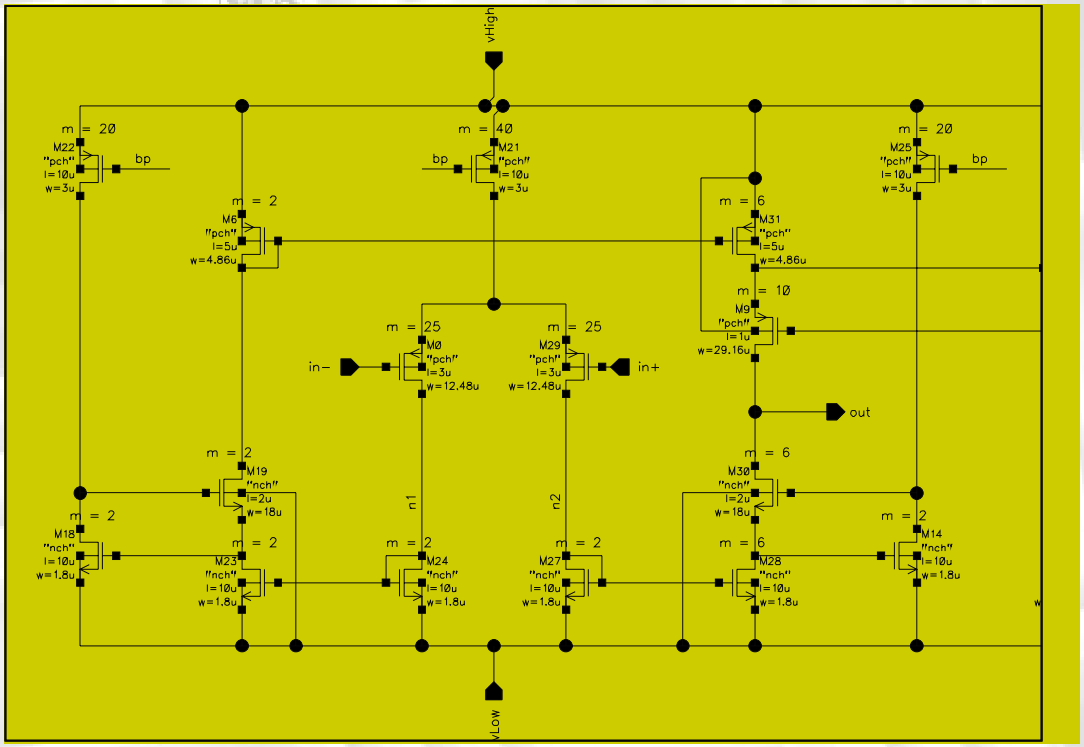
Explanation of voltage drift

- Leakage current in simple diode layout is affected by charge trapped in field oxide above diode
  (hypothesis was verified in $\frac{1}{4}$ micron test circuit)
  - Solutions:
    - Increase diode current (to reduce ratio $I_{leakage}/I_{useful}$)
    - Modify diode perimeter/area ratio

OTA results

- Two stages, double cascoded configuration with PMOS input devices
- Supply current ~ 20 μA
- Output range:
  1 V @ V_{DD} of 1.5 V

- Offset voltage not affected by radiation



Conclusions

- First sub-1 V reference cell with configurable output voltage implemented in 130 nm CMOS
- Functionality OK, but performance degraded due to imprecise process parameters
- Extremely good radiation resistance after 120 Mrad even without enclosed N-channel devices
- New version to be submitted in MPW run at the end of '03